REMARKS/ARGUMENTS

Responsive to the objections against the drawings, the limitation coplanar has been deleted out of claims 1 and 12. Note that Figs. 4, 6, 11 and at least Fig. 11 show source electrode 31, 101, drain electrode 32, 103, and gate electrode 34, 104 according to claims 1 and 12. Withdrawal of the objections is requested.

Responsive to the rejection of claims under 35 U.S.C. §112, first paragraph, note that the Figures now support source, drain and gate electrodes as recited in the claims.

Also, note that the specification at page 7, lines 7-13, discloses a current path that includes vertical portions along gate oxide layers 70 to 74 and "upwardly" through regions 90 or 92 to drain electrode 31. Thus, there is adequate support for the limitations set forth in claims 1, 12 and 27.

Furthermore, Fig. 4 illustrates a P region 51 to which drain electrode 32 is connected, and an N region 52 formed in P region 51 to which source electrode 31 is connected. Thus, Fig. 4 illustrates a PN junction (junction of regions 51, 52) to which drain and source electrodes are connected as recited in the claims.

Responsive to the rejection of claim 27 under 35 U.S.C. §112, first paragraph, the limitation "located outside said region of one conductivity type" has been deleted. Note that Figs. 2 and 8 illustrate two examples of a drain electrode as claimed by claim 27.

In view of the foregoing, reconsideration of the rejection of claims 1, 12, and 27 is requested.

Responsive to the rejection of claims 1, 12 and 27 under 35 U.S.C. §112, second paragraph, the limitation coplanar has been deleted from the claims. It is respectfully submitted that the rejection should now be withdrawn. Reconsideration is requested.

Claims 1, 12 and 27 have been rejected under 35 U.S.C. §103(a) as obvious over Nakagawa et al. (Nakagawa), U.S. 5,105,243, Coe et al. (Coe) U.S. 5,128,730 and Rinne et al. (Rinne) U.S. 6,117,799. Reconsideration is requested.

Claim 1 calls for the following combination:

> 1. A flip chip semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced and metallized layers formed on said first major surface and each connected to one of said P region and said N region; a bottom metallized layer extending across said second major surface; and
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> a third metallized layer atop said first major surface which is laterally spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

Claim 12 calls for the following combination:

> 12. A flip chip semiconductor device comprising a silicon wafer having first and second parallel major surfaces; at least one P region and at least one N region in said wafer which meet at a PN junction within said silicon wafer; first and second laterally spaced metallized layers formed on said first major surface and each connected to one of said P region and said N region; a third metallized layer atop said first major surface which is laterally

spaced from said first and second metallized layers; said first, second and third metallized layers comprising source, drain and gate electrodes respectively of a MOSgated device; and a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to said second metallized layer being aligned along a second straight row, wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface.

Claim 27 call for the following combination:

27. A semiconductor device comprising a silicon die having first and second parallel surfaces; a region of one conductivity type extending from said first surface and into the body of said die; a junction pattern defined in said device formed by a plurality of laterally spaced diffusions of the other conductivity type into said region of one conductivity type; a first conductive power electrode formed atop said first surface and in contact with said plurality of laterally spaced diffusions; a second conductive power electrode formed atop said first surface which is laterally spaced from said first conductive electrode and in electrical contact with the body of said die through a high conductivity element; and at least one solder ball connector formed atop each of said first and second conductive electrodes respectively; the current path inside said silicon die from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface.

It has been alleged that Nakagawa teaches "a current path from said source electrode to said drain electrode [that] includes a vertical component which is generally perpendicular to said first major surface (since Nakagawa et al. teach an electrode 14 located on the second major surface of the device)".

It is respectfully submitted that the claims should be read carefully. As presently worded the claims call for the current path between the power electrodes (source and drain electrodes) that are on the same surface to have a vertical component. The Examiner alleges that Nakagawa teaches a vertical current path between electrodes on opposite surfaces of a die. Clearly, the limitation in question does not read on Nakagawa. Thus, Nakagawa fails to teach the limitation necessary to establish a *prima facie* case of obviousness. Reconsideration is requested.

Each of the remaining claims depends from one of claims 1, 12 and 27, and, therefore, includes the limitations thereof, as well as additional limitations which in combination with those of its base claim are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

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